PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number
18602-08301

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on _____

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Application Number	Filed
10/667,241	September 18,2003
First Named Inventor	
Kevin M. Christiansen	
Art Unit	**Examiner**
2182	Eron J. Sorrell

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.

☒ attorney or agent of record.
Registration number 57,219.

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

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January 18, 2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of one form is submitted.

REMARKS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW IN U.S. PATENT APPLICATION NO. 10/667,241 FILED ON SEPTEMBER 18, 2003

Pre-appeal brief review is appropriate in this application because the rejections in the Final Office Action dated September 18, 2007 contain clear deficiencies. Applicants request that the rejections of claims 21-36 be withdrawn. As set forth below, these rejections are deficient because the cited references fail to include any teaching or suggestion of one or more claim limitations.

REJECTION OF CLAIMS 21-36 UNDER 35 USC 102

Claims 21-36 were rejected under 35 USC §103(a) as allegedly being unpatentable in view of U.S. Patent No. 5,584,010 to Kawai et al. ("Kawai") and U.S. Patent No. 5,614,685 to Matsumoto et al. ("Matsumoto"). This rejection is respectfully traversed.

Independent Claim 21 recites, "a register that stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer." Independent claim 26 similarly recites "means for storing a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer system." Similarly, independent claim 30 recites "a memory configured to store status data generated by an Input/Output (I/O) device after a data unit transfer between the computer system memory and a system external to the computer system." Kawai does not disclose any of these limitations. Rather, Kawai is directed to a multi-processor system having multiple digital signal processors (DSPs). Each DSP has an internal memory but the multi-processor system also includes an "external data memory" outside of the DSPs, which the DSPs access through a main data bus (Kawai, FIG. 5; col. 6, lines 65 to col. 7, line 24). Kawai does not disclose "transfers [of] a data unit to a system" "external to the computer system" or "external to the computer," as claimed. Rather, Kawai merely uses the term "external" to refer to the main memory of the multi-processor system.

Kawai provides no disclosure of a status register that "stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer." Rather, the status register merely indicates whether various DSPs are in a direct memory access mode and whether different DSPs are transmitting or receiving data within the multiprocessor device (Kawai, col. 9, lines 12-20). Therefore, Kawai fails to disclose a register or other storage device which "stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer," as claimed.

Matsumoto fails to remedy the deficiencies of Kawai. There is no indication in Matsumoto that the "external data memory" is external to the DSP. As there is no disclosure in Matsumoto that the DSP communicates with a system external to the musical tone signal processing device, there is no disclosure in Matsumoto of "a register that stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer" or "storing a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer system," as claimed.

Further, Matsumoto also fails to disclose a register or other storage device which "stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer." Neither the I/O control portion nor the DSP in Matsumoto store "a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer," as claimed.

Further, independent claim 34 recites a data transmission method comprising:

> transferring a data unit between a memory in a computer system and a system external to the computer system using a memory access controller coupled to a memory and an Input/Output (I/O) device;
>
> generating status data using the I/O device, the status data indicating completion of the data unit transfer; and
>
> storing the status data in the memory.

As claim 34 similarly recites storing status data after completing a data unit transfer to a system external to the computer system, the above discussion regarding the deficiencies of Kawai and Matsumoto is hereby incorporated so as to apply to claim 30.

By failing to provide any references that disclose or suggest "a register that stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer," "means for storing a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer system," or "a memory configured to store status data generated by an Input/Output (I/O) device after a data unit transfer between the computer system memory and a system external to the computer system" as variously recited in independent claims 21, 26 and 30, the Examiner has failed to establish a *prima facie* case of obviousness and therefore these rejections are improper.

Similarly, by failing to provide any references that disclose or suggest "transferring a data unit between a memory in a computer system and a system external to the computer system using a memory access controller coupled to a memory and an Input/Output (I/O) device," "generating status data using the I/O device, the status data indicating completion of the data unit transfer" and "storing the status data in the memory," as recited in claim 34, the Examiner has failed to establish a *prima facie* case of obviousness and therefore this rejection is improper.

As dependent claims 22-25, 27-29, 31-33, 35 and 36 include the limitations of their respective base claims, the rejections of these claims are also improper.

Respectfully submitted,

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Dated: January 18, 2008

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18602/08301/DOCS/1843423.1